Claims

What is claimed is:

1. A method of integrating a personal computing system, the method comprises the steps of:

a) integrating a central processing unit with a north bridge on to a single substrate such that the central processing unit is directly coupled to the north bridge via an internal bus;

b) providing memory access requests from the central processing unit to the north bridge at a rate of the central processing unit;

c) buffering, in the north bridge, the memory access requests; and

d) processing, by the north bridge, the memory access requests at a rate of memory.

2. The method of claim 1 further comprises:

integrating a south bridge on to the substrate with the central processing unit and the north bridge;

buffering, in the north bridge, memory access requests from the south bridge; and

processing, by the north bridge, the memory access requests from the south bridge at the rate of the memory.

3. The method of claim 1 further comprises:

integrating the memory on to the substrate with the central processing unit and the north bridge.

4. The method of claim 1 further comprises:

integrating a graphics controller on the substrate with the central processing unit and the north bridge;

providing, by the graphics controller, memory access requests for graphics data to the north bridge at a rate of the graphics controller ;

buffering, by the north bridge, the memory access requests for the graphics data;

processing, by the north bridge, the memory access requests for the graphics data at the rate of the memory; and

bypassing an AGP requests and transforming them into memory requests.

5. The method of claim 1 further comprises generating the memory access requests to include an address in physical memory space.

6. The method of claim 1 further comprises:

generating the memory access requests to include an address in virtual memory address space; and

translating, by the north bridge, the address from the virtual memory space to an address in physical memory space.

7. An integrated personal computing system comprises:

a central processing unit operable to execute operational instructions, wherein the central processing unit includes an arithmetic logic unit interoperably coupled with a data module (cache and cache management module), an instruction module (cache, fetch module, decoder, and cache management module), and a programmable phase locked loop that provides an operating rate for the central processing unit, wherein the central processing unit issues a memory access request when information relating to executing one of the operational instructions is not stored within the data module or the instruction module, and wherein the central processing unit is contained on a substrate;

north bridge operably coupled to interface with memory at a memory rate, wherein the north bridge includes a memory access request buffer interoperably coupled with a memory controller, wherein the memory access request buffer receives the memory access request from the central processing unit at the operating rate of the central processing unit, wherein the memory controller retrieves the memory access request from the memory access request buffer at the memory rate, wherein the memory controller processes the memory access request to produce a memory response that includes the information, and wherein the north bridge is contained on the substrate; and

a bus operably coupled to the central processing unit and the north bridge, wherein the bus provides a transport medium for memory access requests and corresponding memory responses between the central processing unit and the north bridge at the operating rate of the central processing unit, and wherein the bus is contained on the substrate.

8. The integrated personal computing system of claim 7, wherein the data module further comprises operable coupling to a data portion of the bus, wherein the data module provides data memory access requests via the data portion of the bus to the north bridge and wherein the memory access request buffer further comprises a data portion operably coupled to receive the data memory access requests from the data portion of the bus.

9. The integrated personal computing system of claim 7, wherein the instruction module further comprises operable coupling to an instruction portion of the bus, wherein the instruction module provides instruction memory access requests via the instruction portion of the bus to the north bridge and wherein the memory access request buffer further comprises an instruction portion operably coupled to receive the instruction memory access requests from the instruction portion of the bus.

10. The integrated personal computing system of claim 7, wherein the central processing unit further comprises an address generation unit that generates the memory access request to include an address in physical memory space.

11. The integrated personal computing system of claim 7 further comprises:

a memory bus that is contained on the substrate, wherein the memory bus couples the north bridge to the memory, and wherein the memory is contained on the substrate.

12. The integrated personal computing system of claim 7 further comprises:

a device bus that is contained on the substrate, wherein the device bus couples the north bridge to south bridge that is contained on the substrate.

13. The integrated personal computing system of claim 7 further comprises: a graphics controller that is contained on the substrate, wherein the graphics controller includes a frame buffer controller for processing data transferences between the graphics controller and a frame buffer and wherein the graphics controller issues a graphics memory access request to the north bridge.

14. An integrated memory system comprises:

memory that is contained on a substrate;

north bridge operably coupled to interface with the memory at a memory rate, wherein the north bridge includes a memory access request buffer interoperably coupled with a memory controller, wherein the memory access request buffer receives a memory access request, wherein the memory controller retrieves the memory access request from the memory access request buffer at the memory rate, wherein the memory controller processes the memory access request to produce a memory response, and wherein the north bridge is contained on the substrate; and

a memory bus operably coupled to the memory and the north bridge, wherein the memory bus is contained on the substrate.

15. The integrated memory system of claim 14 further comprises:

a central processing unit operable to execute operational instructions, wherein the central processing unit includes an arithmetic logic unit interoperably coupled with a data module, an instruction module, and a programmable phase locked loop that provides an operating rate for the central processing unit, wherein the central processing unit issues, at the operating rate of the central processing unit, the memory access request when information relating to executing one of the operational instructions is not stored within the data module or the instruction module, and wherein the central processing unit is contained on the substrate; and

a bus operably coupled to the central processing unit and the north bridge, wherein the bus provides a transport medium for memory access requests and corresponding memory responses between the central processing unit and the north bridge at the operating rate of the central processing unit, and wherein the bus is contained on the substrate.

16. The integrated memory system of claim 15, wherein the central processing unit further comprises an address generation unit that generates the memory access request to include an address in virtual memory address space, and wherein the north bridge further comprises an address translation module operably coupled to translate the address from the virtual memory space to an address in physical memory space.

17. The integrated memory system of claim 15, wherein the central processing unit further comprises an address generation unit that generates the memory access request to include an address in physical memory space.

18. The integrated memory system of claim 14, wherein the north bridge further comprises a PCI bus interface to provide coupling, via a PCI bus, to a device interface module.

19. The integrated memory system of claim 14 further comprises:

a device bus that is contained on the substrate, wherein the device bus couples the north bridge to south bridge that is contained on the substrate.

20. An integrated personal computing system comprises:

a central processing unit operable to execute operational instructions, wherein the central processing unit includes an arithmetic logic unit interoperably coupled with a data module (cache and cache management module), an instruction module (cache, fetch module, decoder, and cache management module), and a programmable phase locked loop that provides an operating rate for the central processing unit, wherein the central processing unit issues a memory access request when information relating to executing one of the operational instructions is not stored within the data module or the instruction module, and wherein the central processing unit is contained on a substrate;

north bridge operably coupled to interface with memory at a memory rate, wherein the north bridge includes a memory access request buffer interoperably coupled with a memory controller, wherein the memory access request buffer receives the memory access request from the central processing unit at the operating rate of the central processing unit, wherein the memory controller retrieves the memory access request from the memory access request buffer at the memory rate, wherein the memory controller processes the memory access request to produce a memory response that includes the information, and wherein the north bridge is contained on the substrate;

a bus operably coupled to the central processing unit and the north bridge, wherein the bus provides a transport medium for memory access requests and corresponding memory responses between the central processing unit and the north bridge at the operating rate of the central processing unit, and wherein the bus is contained on the substrate;

south bridge that is contained on the substrate, wherein the south bridge provides an interface between at least one external device and the north bridge; and

a device bus that is contained on the substrate, wherein the device bus couples the north bridge to the south bridge.

21. The integrated personal computing system of claim 20, wherein the data module further comprises operable coupling to a data portion of the bus, wherein the data module provides data memory access requests via the data portion of the bus to the north bridge and wherein the memory access request buffer further comprises a data portion operably coupled to receive the data memory access requests from the data portion of the bus.

22. The integrated personal computing system of claim 20, wherein the instruction module further comprises operable coupling to an instruction portion of the bus, wherein the instruction module provides instruction memory access requests via the instruction portion of the bus to the north bridge and wherein the memory access request buffer further comprises an instruction portion operably coupled to receive the instruction memory access requests from the instruction portion of the bus.

23. The integrated personal computing system of claim 20, wherein the central processing unit further comprises an address generation unit that generates the memory access request to include an address in physical memory space.

24. The integrated computing system of claim 20, wherein the central processing unit further comprises an address generation unit that generates the memory access request to include an address in virtual memory address space, and wherein the north bridge further comprises an address translation module operably coupled to translate the address from the virtual memory space to an address in physical memory space.

25. The integrated computing system of claim 20, wherein the north bridge further comprises a memory bus interface to provide coupling, via a memory bus, to the memory.

26. The integrated computing system of claim 20 further comprises:

a memory bus that is contained on the substrate, wherein the memory bus couples the north bridge to the memory, and wherein the memory is contained on the substrate.

27. The integrated computing system of claim 20 further comprises a device bus arbitrator that arbitrates allocation of the device bus among a plurality of device interfacing modules within the south bridge.

28. A method of integrating a personal computing system, the method comprises the steps of:

a) integrating a central processing unit with a north bridge and a south bridge on to a single substrate such that the central processing unit is directly coupled to the north bridge via an internal bus;

b) providing memory access requests from the central processing unit to the north bridge at a rate of the central processing unit;

c) buffering, in the north bridge, the memory access requests; and

d) processing, by the north bridge, the memory access requests at a rate of memory.

29. The method of claim 28 further comprises:

buffering, in the north bridge, memory access requests from the south bridge; and

processing, by the north bridge, the memory access requests from the south bridge at the rate of the memory.

30. The method of claim 28 further comprises:

integrating the memory on to the substrate with the central processing unit and the north bridge.

31. The method of claim 28 further comprises:

integrating a graphics controller on the substrate with the central processing unit and the north bridge;

providing, by the graphics controller, memory access requests for graphics data to the north bridge at a rate of the graphics controller;

buffering, by the north bridge, the memory access requests for the graphics data; and

processing, by the north bridge, the memory access requests for the graphics data at the rate of the memory.

32. The method of claim 28 further comprises generating the memory access requests to include an address in physical memory space.

33. The method of claim 28 further comprises:

generating the memory access requests to include an address in virtual memory address space; and

translating, by the north bridge, the address from the virtual memory space to an address in physical memory space.